Docket No.: END919970075US3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Kresge et al.

Group Art Unit:	:	IBM Corporation
Examiner:	:	Intellectual Property Law
Serial No.:	:	Dept. N50, Bldg. 040-4
Filed: Herewith	:	1701 North Street
Title: ELECTRONIC PACKAGE FOR ELECTRONIC COMPONENTS AND METHOD OF MAKING SAME	:	Endicott, NY 13760

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(Date of Deposit)

June M. Mitchell 1/7/02

June M. Mitchell Date

Assistant Commissioner For Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the above-identifed application as follows:

In the Specification:

Page 1, line 7 - before "Background of the Invention", please add:

--Cross Reference to Copending Application

This application is a divisional application of S.N. 09/346,356, filed 07/02/99.--

In the Claims:

Please cancel all the claims and add the following new claims:

--80. A method of making a multi-layered interconnect structure adapted for electrically interconnecting a semiconductor chip and a circuitized substrate using solder connections, said method comprising the steps of:

providing a thermally conductive layer including first and second opposing surfaces;

positioning first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively; and

positioning first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a semiconductor chip and a circuitized substrate, respectively, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate.

81. The method of making the multi-layered interconnect structure of claim 80 wherein said step of positioning said first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively, comprises laminating said first and second dielectric layers onto said first and second opposing

surfaces at a pressure of from about 1000 to about 1500 psi and at a temperature of from about 600 to about 750 °F.

82. The method of making the multi-layered interconnect structure of claim 80 wherein said positioning said first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, comprises the steps of:

laminating a copper foil onto said first and second dielectric layers; and

etching selected portions of said copper foil to produce first and second pluralities of said electrically conductive members.

83. The method of making the multi-layered interconnect structure of claim 80 further including the steps of:

positioning a third dielectric layer on said first dielectric layer and on said first plurality of electrically conductive members;

removing portions of said third dielectric layer to expose portions of said first plurality of electrically conductive members; and

forming a first plurality of microvias within said third dielectric layer to expose at least a portion of at least one of said first plurality of electrically conductive members.

84. The method of making the multi-layered interconnect structure of claim 83 wherein said removing of said portions of said third dielectric layer is performed by laser ablating.

85. The method of making the multi-layered interconnect structure of claim 80 further including the steps of:

positioning a fourth dielectric layer on said second dielectric layer and on said second plurality of electrically conductive members;

removing portions of said fourth dielectric layer to expose portions of said second plurality of electrically conductive members; and

forming a second plurality of microvias within said fourth dielectric layer to expose at least a portion of at least one of said second plurality of electrically conductive members.

86. The method of making the multi-layered interconnect structure of claim 85 wherein the step of removing portions of said fourth dielectric layer is performed by laser ablating.

87. A method of making an electronic package comprising the steps of:

providing a semiconductor chip having a first surface including a plurality of contact sites thereon;

providing a multi-layered interconnect structure adapted for electrically interconnecting said semiconductor chip to a circuitized substrate, said multi-layered interconnect structure including a thermally conductive layer, having first and second opposing surfaces, first and second dielectric layers positioned on said first and second opposing surfaces, respectively, and first and second pluralities of electrically conductive members positioned on said first and second dielectric layers, respectively;

providing a first plurality of solder connections on said first plurality of electrically conductive members; and

connecting respective ones of said first plurality of solder connections to respective ones of said plurality of contact sites on said semiconductor chip, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip.

88. The method of making the electronic package of claim 87 wherein said step of providing said first plurality of solder connections on said first plurality of electrically conductive members includes:

forming a plurality of openings in said third dielectric layer, each of said openings including an internal wall and exposing a portion of at least one of said first plurality of electrically conductive members;

plating a conductive layer on said internal wall of said plurality of openings and on said exposed portion of said at least one of said first plurality of electrically conductive members to define a plurality of microvias;

applying a first solder paste onto said conductive layer; and

reflowing said solder paste to form a first plurality of solder connections.

89. The method of making the electronic package of claim 88 wherein said step of connecting respective ones of said first plurality of solder connections to respective ones of said plurality of contact members on said semiconductor chip further includes the steps of applying a second solder paste onto said respective ones of said first plurality of solder connections, positioning said respective ones of said contact members of said semiconductor chip against said respective ones of said first plurality of solder connections, and reflowing said second solder paste and said respective ones of said first plurality of solder connections to electrically connect said semiconductor chip to said multi-layered interconnect structure.

90. The method of making the electronic package of claim 87 further including the steps of:

providing a circuitized substrate having a first surface including a plurality of contact pads thereon;

providing a second plurality of solder connections on said second plurality of conductive members of said multi-layered interconnect structure; and

connecting respective ones of said second plurality of said solder connections to respective ones of said plurality of contact pads on said circuitized substrate to make electrical connections therebetween.

91. A method of making a multi-layered interconnect structure adapted for electrically interconnecting a semiconductor chip and a circuitized substrate using solder connections, said method comprising the steps of:

providing a thermally conductive layer including first and second opposing surfaces;

positioning first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively;

positioning a first electrically conductive layer within said first dielectric layer;

positioning a second electrically conductive layer between said first electrically conductive layer and said thermally conductive layer wherein said second electrically conductive layer comprises a first plurality of shielded signal conductors; and

positioning first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a semiconductor chip and a circuitized substrate, respectively, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate.

92. The method of making the multi-layered interconnect structure of claim 91 wherein said step of positioning said first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively, comprises laminating said first and second dielectric layers onto said first and second opposing surfaces at a pressure of from about 1000 to about 1500 psi and at a temperature of from about 600 to about 750 ° F.

93. The method of making the multi-layered interconnect structure of claim 91 wherein said positioning said first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, comprises the steps of:

laminating a copper foil onto said first and second dielectric layers; and

etching selected portions of said copper foil to produce first and second pluralities of said electrically conductive members.

94. The method of making the multi-layered interconnect structure of claim 91 further including the steps of:

positioning a third dielectric layer on said first dielectric layer and on said first plurality of electrically conductive members;

removing portions of said third dielectric layer to expose portions of said first plurality of electrically conductive members; and

forming a first plurality of microvias within said third dielectric layer to expose at least a portion of at least one of said first plurality of electrically conductive members.

95. The method of making the multi-layered interconnect structure of claim 94 wherein said removing of said portions of said third dielectric layer is performed by laser ablating.

96. The method of making the multi-layered interconnect structure of claim 91 further including the steps of:

positioning a fourth dielectric layer on said second dielectric layer and on said second plurality of electrically conductive members;

removing portions of said fourth dielectric layer to expose portions of said second plurality of electrically conductive members; and

forming a second plurality of microvias within said fourth dielectric layer to expose at least a portion of at least one of said second plurality of electrically conductive members.

97. The method of making the multi-layered interconnect structure of claim 96 wherein the step of removing portions of said fourth dielectric layer is performed by laser ablating.--

REMARKS

The specification is amended to reference the parent application, S/N 09/346,356.

Claims 1-79 are cancelled. Claims 80-97, directed to Applicant's method, and withdrawn in the parent application, have been added.

New independent method claim 80 recites the subject matter of original independent method claim 69.

New dependent method claims 81-86 recite the subject matter of original dependent claims 70-75, and depend from new independent claim 80.

New independent method claim 87 recites the subject matter of original independent claim 76. New dependent claims 88-90 recite the subject matter of original dependent claims 77-79 and depend from new independent method claim 87.

New independent method claim 91 recites the subject matter of original independent method claim 69 and includes the steps of positioning a first electrically conductive layer within the first dielectric layer, and positioning a second electrically conductive layer between the first electrically conductive layer and the thermally conductive layer wherein the second electrically conductive layer comprises a first plurality of shield signal conductors. Support is found on page 7, lines 10-17 and lines 23-24.

New dependent method claims 92-97 recite the subject matter of original dependent claims 70-75 and depend from new independent method claim 91.

Support being provided for all the above amending, this amending does not constitute the addition of new matter and entry is urged.

Attached hereto is a marked up version of the changes made to the specification by the current amendment. This page is captioned Version with markings to show changes made.

Copies of the IDS and PTO-1449 form mailed on 08/12/99 and Supplemental IDS and PTO-1449 forms mailed on 09/29/99, 07/05/00, and 08/21/01 in the parent application, S.N. 09/346,356, are included herewith. Upon request, copies of the documents cited in the IDSs and PTO-1449 forms will be provided.

The Application is deemed in condition for allowance and such action by the Examiner is urged. Should differences remain, however, which do not place one/more of the remaining claims in condition for allowance, the Examiner is requested to phone the undersigned at the number provided below for the purpose of providing constructive assistance and suggestions in accordance with M.P.E.P. Sections 707, 707.07(d) and 707.07(j) in order that allowable claims can be presented, thereby placing the application in condition for allowance without further proceedings being necessary.

Respectfully submitted,

Dated: Jan. 07, 2002

By: _____
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Version with markings to show changes made

ELECTRONIC PACKAGE FOR ELECTRONIC COMPONENTS AND METHOD OF MAKING SAME

TECHNICAL FIELD

The present invention relates, in general, to an electronic package for mounting of integrated circuits, and in particular, to an organic multi-layered interconnect structure for use in such a package.

Added "Cross Reference to Copending Application"

BACKGROUND OF THE INVENTION

Organic substrates for example printed circuit boards and chip carriers have been and continue to be developed for many applications. These are expected to displace ceramic substrates, in particular in many chip carrier applications, because of reduced cost and enhanced electrical performance. The use of a multi-layered interconnect structure such as an organic chip carrier for interconnecting a semiconductor chip to a printed circuit board in an electronic package introduces many challenges, one of which is the reliability of the connection joints between the semiconductor chip and the organic chip carrier and another of which is the reliability of the connection joints between the organic chip carrier and the printed circuit board.

As semiconductor chip input/output (I/O) counts increase beyond the capability of peripheral lead devices and as the need for both semiconductor chip and printed circuit board miniaturization increases, area array interconnects are the preferred method for making large numbers of connections between a semiconductor chip and an organic chip carrier and between the organic chip carrier and a printed circuit board. If the coefficient of thermal expansion (CTE) of the semiconductor chip, the organic chip carrier, and the printed circuit board are substantially different from one another, industry standard semiconductor chip array interconnections to the organic chip carrier can exhibit high stress during operation (thermal cycling). Similarly, the industry standard ball grid array (BGA) interconnections between the organic chip carrier and